

## FEATURES

- Vcc operation voltage: 2.4V ~ 5.5V
- Very low power consumption
  - Vcc = 3.0V C-grade: 11mA (@55ns) operating current  
I-grade: 12mA (@55ns) operating current  
C-grade: 9mA (@70ns) operating current  
I-grade: 10mA (@70ns) operating current  
18uA(Typ.) CMOS standby current
  - Vcc = 5.0V C-grade: 12mA (@55ns) operating current  
I-grade: 13mA (@55ns) operating current  
C-grade: 10mA (@70ns) operating current  
I-grade: 11mA (@70ns) operating current  
18uA(Typ.) CMOS standby current
- High speed access time:
  - 55 55ns (Max.) @ Vcc: 3.0~5.5V
  - 70 70ns (Max.) @ Vcc: 2.7~5.5V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Data retention supply voltage as low as 1.5V
- Easy expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- I/O Configuration x8/x16 selectable by LB and UB pin

## DESCRIPTION

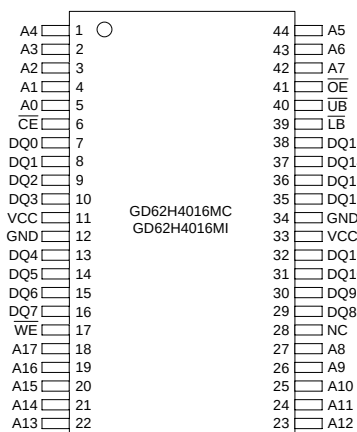
The GD62H4016 is a high performance, very low power CMOS Static Random Access Memory organized as 262,144 by 16 bits and operates from a range of 2.4V to 5.5V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with maximum operation current of 12mA at 3.0V and access time of 55ns. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state output drivers. The GD62H4016 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The GD62H4016 is available in DICE form, JEDEC standard 44 pin Plastic TSOP Type II.

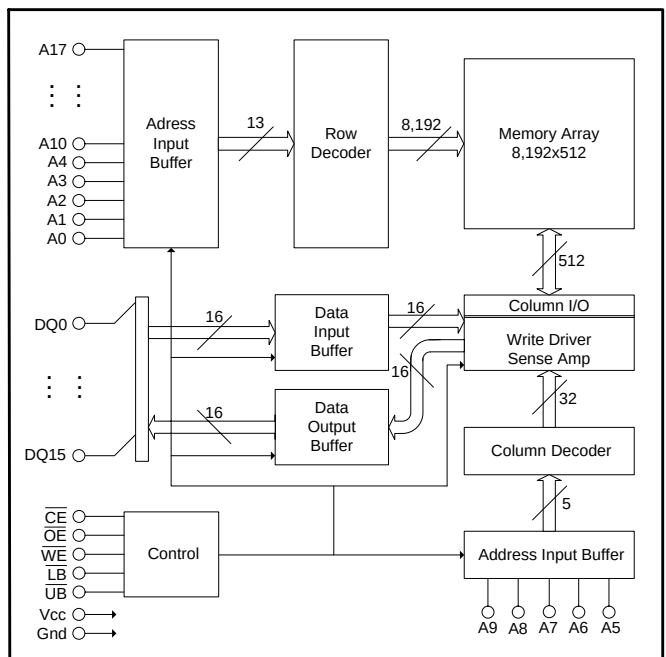
## PRODUCT FAMILY

| PRODUCT FAMILY | OPERATING TEMPERATURE         | POWER DISSIPATION |          |          |          |                 |          | PACKAGE |
|----------------|-------------------------------|-------------------|----------|----------|----------|-----------------|----------|---------|
|                |                               | OPERATING CURRENT |          |          |          | STANDBY CURRENT |          |         |
|                |                               | (Max, mA)         |          |          |          | (Typ., uA)      |          |         |
|                |                               | 55ns              |          | 70ns     |          |                 |          |         |
|                |                               | Vcc=3.0V          | Vcc=5.0V | Vcc=3.0V | Vcc=5.0V | Vcc=3.0V        | Vcc=5.0V |         |
| GD62H4016NC    | Commercial<br>0°C to +70°C    | 11                | 12       | 9        | 10       | 18              | 18       | DICE    |
| GD62H4016MC    |                               | TSOP II -44       |          |          |          |                 |          |         |
| GD62H4016NI    | Industrial<br>-40°C to +85 °C | 12                | 13       | 10       | 11       | 18              | 18       | DICE    |
| GD62H4016MI    |                               | TSOP II -44       |          |          |          |                 |          |         |

## PIN CONFIGURATIONS



## BLOCK DIAGRAM



## PIN DESCRIPTIONS

| NAME                                                        | FUNCTION                                                                                                                                                                                                                                                                                                                  |
|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0-A17 Address Input                                        | These 18 address inputs select one of the 262,144 x 16-bit in the RAM                                                                                                                                                                                                                                                     |
| $\overline{CE}$ Chip Enable Input                           | $\overline{CE}$ is active LOW, chip enables must be active when data read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.                                              |
| $\overline{WE}$ Write Enable Input                          | The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location. |
| $\overline{OE}$ Output Enable Input                         | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive                                         |
| $\overline{LB}$ and $\overline{UB}$ Data Byte Control Input | Lower byte and upper byte data from or write data into the RAM                                                                                                                                                                                                                                                            |
| DQ0-DQ15 Data Input/Output Ports                            | These 16 bi-directional ports are used to read data from or write data into the RAM                                                                                                                                                                                                                                       |
| Vcc                                                         | Power Supply                                                                                                                                                                                                                                                                                                              |
| Gnd                                                         | Ground                                                                                                                                                                                                                                                                                                                    |

## TRUTH TABLE

| MODE                             | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | DQ0~DQ7          | DQ8~DQ15         | Vcc CURRENT           |
|----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-----------------------|
| Chip De-selected<br>(Power Down) | H               | X               | X               | X               | X               | High Z           | High Z           | $I_{CCSB}, I_{CCSB1}$ |
|                                  | X               | X               | X               | H               | H               | High Z           | High Z           | $I_{CCSB}, I_{CCSB1}$ |
| Output Disabled                  | L               | H               | H               | L               | X               | High Z           | High Z           | $I_{CC}$              |
|                                  | L               | H               | H               | X               | L               | High Z           | High Z           | $I_{CC}$              |
| Read                             | L               | H               | L               | L               | L               | D <sub>OUT</sub> | D <sub>OUT</sub> | $I_{CC}$              |
|                                  |                 |                 |                 | H               | L               | High Z           | D <sub>OUT</sub> | $I_{CC}$              |
|                                  |                 |                 |                 | L               | H               | D <sub>OUT</sub> | High Z           | $I_{CC}$              |
| Write                            | L               | L               | X               | L               | L               | D <sub>IN</sub>  | D <sub>IN</sub>  | $I_{CC}$              |
|                                  |                 |                 |                 | H               | L               | X                | D <sub>IN</sub>  | $I_{CC}$              |
|                                  |                 |                 |                 | L               | H               | D <sub>IN</sub>  | X                | $I_{CC}$              |

## ABSOLUTE MAXIMUM RATINGS\*

| SYMBOL            | PARAMETER                            | RATING      | UNITS |
|-------------------|--------------------------------------|-------------|-------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | -0.5 to 7.0 | V     |
| T <sub>BIAS</sub> | Temperature Under Bias               | -40 to +125 | °C    |
| T <sub>STG</sub>  | Storage Temperature                  | -60 to +150 | °C    |
| P <sub>T</sub>    | Power Dissipation                    | 1.0         | W     |
| I <sub>OUT</sub>  | DC Output Current                    | 20          | mA    |

## CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0 MHz)

| SYMBOL          | PARAMETER                | CONDITIONS           | MAX. | UNITS |
|-----------------|--------------------------|----------------------|------|-------|
| C <sub>IN</sub> | Input Capacitance        | V <sub>IN</sub> =0V  | 6    | pF    |
| C <sub>DQ</sub> | Input/Output Capacitance | V <sub>I/O</sub> =0V | 8    | pF    |

\* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**

| PARAMETER NAME     | PARAMETER                                    | TEST CONDITIONS                                                                                                                          |                       |      | MIN. | TYP. <sup>(1)</sup> | MAX.                 | UNITS |
|--------------------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|------|---------------------|----------------------|-------|
| V <sub>IL</sub>    | Guaranteed Input Low Voltage <sup>(2)</sup>  |                                                                                                                                          |                       |      | -0.5 | --                  | 0.8                  | V     |
| V <sub>IH</sub>    | Guaranteed Input High Voltage <sup>(2)</sup> |                                                                                                                                          |                       |      | 2.2  | --                  | V <sub>CC</sub> +0.3 | V     |
| I <sub>IL</sub>    | Input Leakage Current                        | V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub> $\overline{CE}$ =V <sub>IH</sub>                                          |                       |      | --   | --                  | 1                    | uA    |
| I <sub>LO</sub>    | Output Leakage Current                       | V <sub>CC</sub> = Max, V <sub>I/O</sub> = 0V to V <sub>CC</sub> $\overline{CE}$ = V <sub>IH</sub> or $\overline{OE}$ = V <sub>IH</sub> , |                       |      | --   | --                  | 1                    | uA    |
| V <sub>OL</sub>    | Output Low Voltage                           | V <sub>CC</sub> = Max, I <sub>OL</sub> = 2.0mA                                                                                           |                       |      | --   | --                  | 0.4                  | V     |
| V <sub>OH</sub>    | Output High Voltage                          | V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0mA                                                                                          |                       |      | 2.4  | --                  | --                   | V     |
| I <sub>CC</sub>    | Operating Power Supply Current               | $\overline{CE}$ = V <sub>IL</sub> ,<br>I <sub>DQ</sub> = 0mA,<br>F = Fmax <sup>(3)</sup>                                                 | V <sub>CC</sub> =3.0V | 70ns | --   | --                  | 9                    | mA    |
|                    |                                              |                                                                                                                                          |                       | 55ns | --   | --                  | 11                   |       |
|                    |                                              |                                                                                                                                          | V <sub>CC</sub> =5.0V | 70ns | --   | --                  | 10                   |       |
|                    |                                              |                                                                                                                                          |                       | 55ns | --   | --                  | 12                   |       |
| I <sub>CCSB</sub>  | Standby Current-TTL                          | $\overline{CE}$ = V <sub>IH</sub> ,<br>I <sub>DQ</sub> = 0mA                                                                             | V <sub>CC</sub> =3.0V |      | --   | --                  | 1.0                  | mA    |
|                    |                                              |                                                                                                                                          | V <sub>CC</sub> =5.0V |      | --   | --                  | 2.0                  |       |
| I <sub>CCSB1</sub> | Standby Current-CMOS                         | $\overline{CE} \geq V_{CC}-0.2V$ ,<br>V <sub>IN</sub> $\geq V_{CC}-0.2V$ or V <sub>IN</sub> $\leq 0.2V$                                  | V <sub>CC</sub> =3.0V |      | --   | 18                  | --                   | uA    |
|                    |                                              |                                                                                                                                          | V <sub>CC</sub> =5.0V |      | --   | 18                  | --                   |       |

1. Typical characteristics are at  $T_A = 25^{\circ}\text{C}$ .

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3.  $F_{\text{MAX}} = 1/t_{RC}$ .

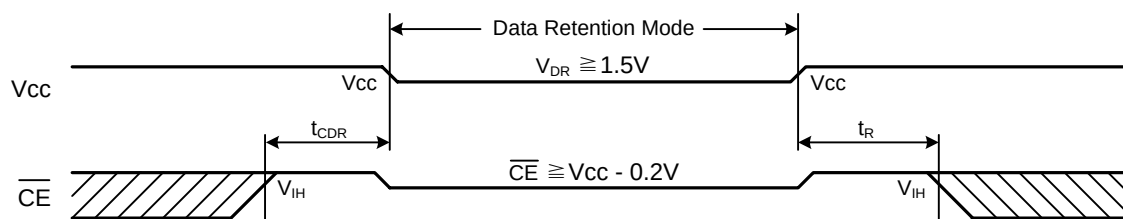
**DATA RETENTION CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**

| PARAMETER NAME | PARAMETER                            | TEST CONDITIONS                                                                                             | MIN.           | TYP. <sup>(1)</sup> | MAX. | UNITS         |
|----------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------|----------------|---------------------|------|---------------|
| $V_{DR}$       | $V_{CC}$ for Data Retention          | $\overline{CE} \geq V_{CC} - 0.2\text{V}$<br>$V_{IN} \geq V_{CC} - 0.2\text{V or } V_{IN} \leq 0.2\text{V}$ | 1.5            | --                  | --   | V             |
| $I_{CCDR}$     | Data Retention Current               | $\overline{CE} \geq V_{CC} - 0.2\text{V}$<br>$V_{IN} \geq V_{CC} - 0.2\text{V or } V_{IN} \leq 0.2\text{V}$ | --             | 15                  | --   | $\mu\text{A}$ |
| $t_{CDR}$      | Chip Deselect to Data Retention Time | See Retention Waveform                                                                                      | 0              | --                  | --   | ns            |
| $t_R$          | Operation Recovery Time              |                                                                                                             | $t_{RC}^{(2)}$ | --                  | --   | ns            |

1.  $V_{CC}=1.5\text{V}, T_A = +25^{\circ}\text{C}$

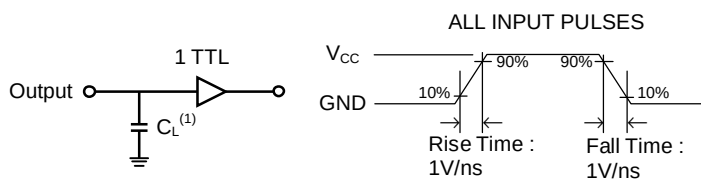
2.  $t_{RC}$  = Read Cycle Time

**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**



### AC TEST CONDITIONS

|                                         |                                               |
|-----------------------------------------|-----------------------------------------------|
| Input Pulse Levels                      | $V_{CC}/0V$                                   |
| Input Rise and Fall Times               | 1V/ns                                         |
| Input and Output Timing Reference Level | 0.5V <sub>CC</sub>                            |
| Output Load                             | $t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}$ |
|                                         | Others                                        |
|                                         | $C_L = 5pF + 1TTL$                            |
|                                         | $C_L = 30pF + 1TTL$                           |



1. Including jig and scope capacitance.

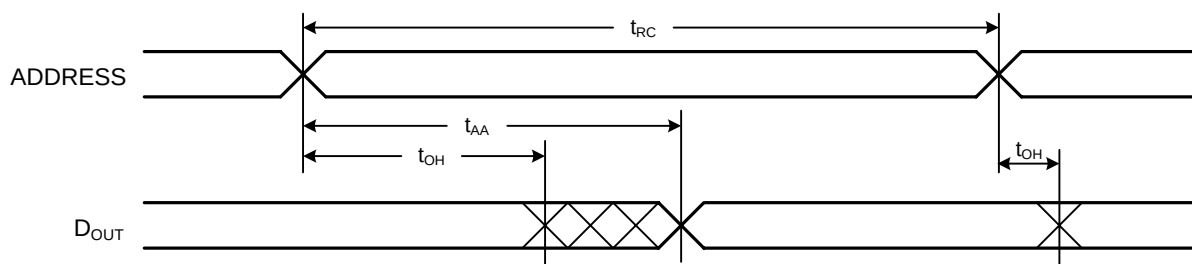
### AC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}C$ to $+85^{\circ}C$ )

#### READ CYCLE

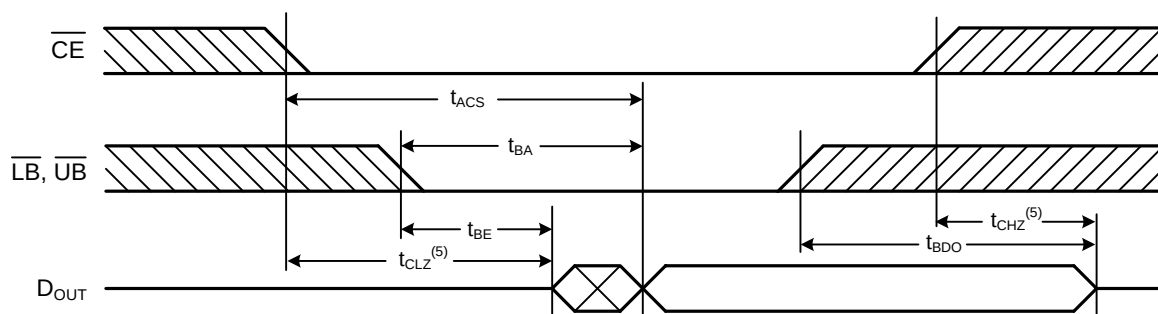
| JEDEC<br>PARAMETER<br>NAME | PARAMETER<br>NAME | DESCRIPTION                                                           | CYCLE TIME :55ns<br>( $V_{CC}=3.0-5.5V$ ) |      |      | CYCLE TIME :70ns<br>( $V_{CC}=2.7-5.5V$ ) |      |      | UNIT |
|----------------------------|-------------------|-----------------------------------------------------------------------|-------------------------------------------|------|------|-------------------------------------------|------|------|------|
|                            |                   |                                                                       | MIN.                                      | TYP. | MAX. | MIN.                                      | TYP. | MAX. |      |
| $t_{AVAX}$                 | $t_{RC}$          | Read Cycle Time                                                       | 55                                        | --   | --   | 70                                        | --   | --   | ns   |
| $t_{AVQV}$                 | $t_{AA}$          | Address Access Time                                                   | --                                        | --   | 55   | --                                        | --   | 70   | ns   |
| $t_{ELQV}$                 | $t_{ACS}$         | Chip Select Access Time ( $\overline{CE}$ )                           | --                                        | --   | 55   | --                                        | --   | 70   | ns   |
| $t_{BLQV}$                 | $t_{BA}$          | Data Byte Control Access Time ( $\overline{LB}, \overline{UB}$ )      | --                                        | --   | 55   | --                                        | --   | 70   | ns   |
| $t_{GLQV}$                 | $t_{OE}$          | Output Enable to Output Valid                                         | --                                        | --   | 30   | --                                        | --   | 35   | ns   |
| $t_{ELQX}$                 | $t_{CLZ}$         | Chip Select to Output Low Z ( $\overline{CE}$ )                       | 10                                        | --   | --   | 10                                        | --   | --   | ns   |
| $t_{BLQX}$                 | $t_{BE}$          | Data Byte Control to Output Low Z ( $\overline{LB}, \overline{UB}$ )  | 10                                        | --   | --   | 10                                        | --   | --   | ns   |
| $t_{GLQX}$                 | $t_{OLZ}$         | Output Enable to Output in Low Z                                      | 5                                         | --   | --   | 5                                         | --   | --   | ns   |
| $t_{EHQZ}$                 | $t_{CHZ}$         | Chip Deselect to Output in High Z ( $\overline{CE}$ )                 | --                                        | --   | 30   | --                                        | --   | 35   | ns   |
| $t_{BHQZ}$                 | $t_{BDO}$         | Data Byte Control to Output High Z ( $\overline{LB}, \overline{UB}$ ) | --                                        | --   | 30   | --                                        | --   | 35   | ns   |
| $t_{GHQZ}$                 | $t_{OHZ}$         | Output Disable to Output in High Z                                    | --                                        | --   | 25   | --                                        | --   | 30   | ns   |
| $t_{AXQX}$                 | $t_{OH}$          | Data Hold from Address Change                                         | 10                                        | --   | --   | 10                                        | --   | --   | ns   |

### SWITCHING WAVEFORMS (READ CYCLE)

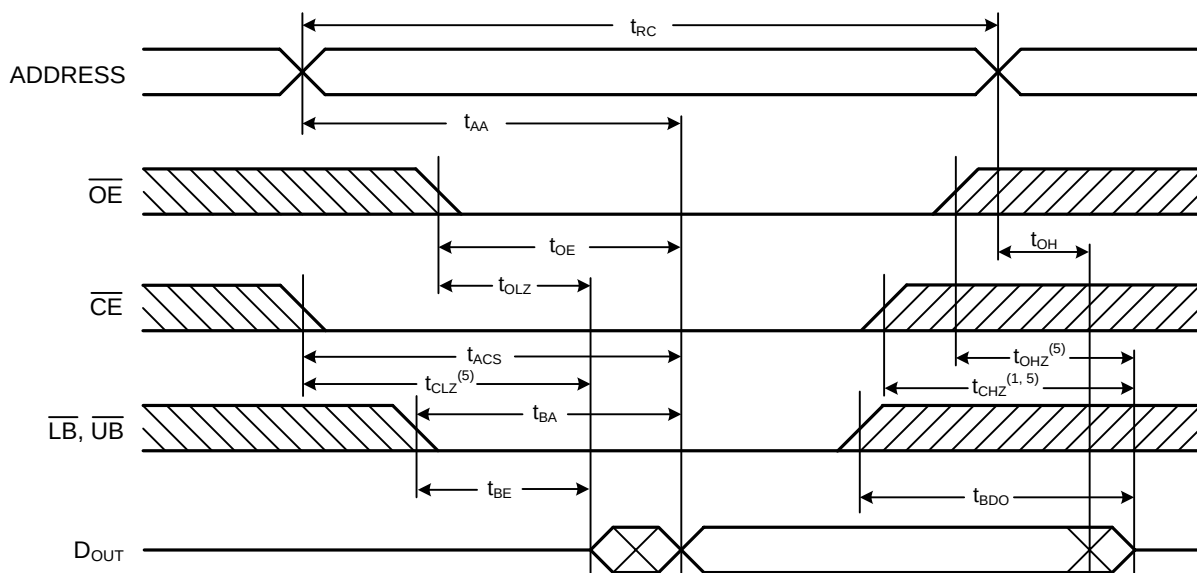
#### READ CYCLE 1 (1, 2, 4)



READ CYCLE 2 <sup>(1, 3, 4)</sup>



READ CYCLE 3 <sup>(1, 4)</sup>



NOTES:

1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ . The parameter is guaranteed but not 100% tested.

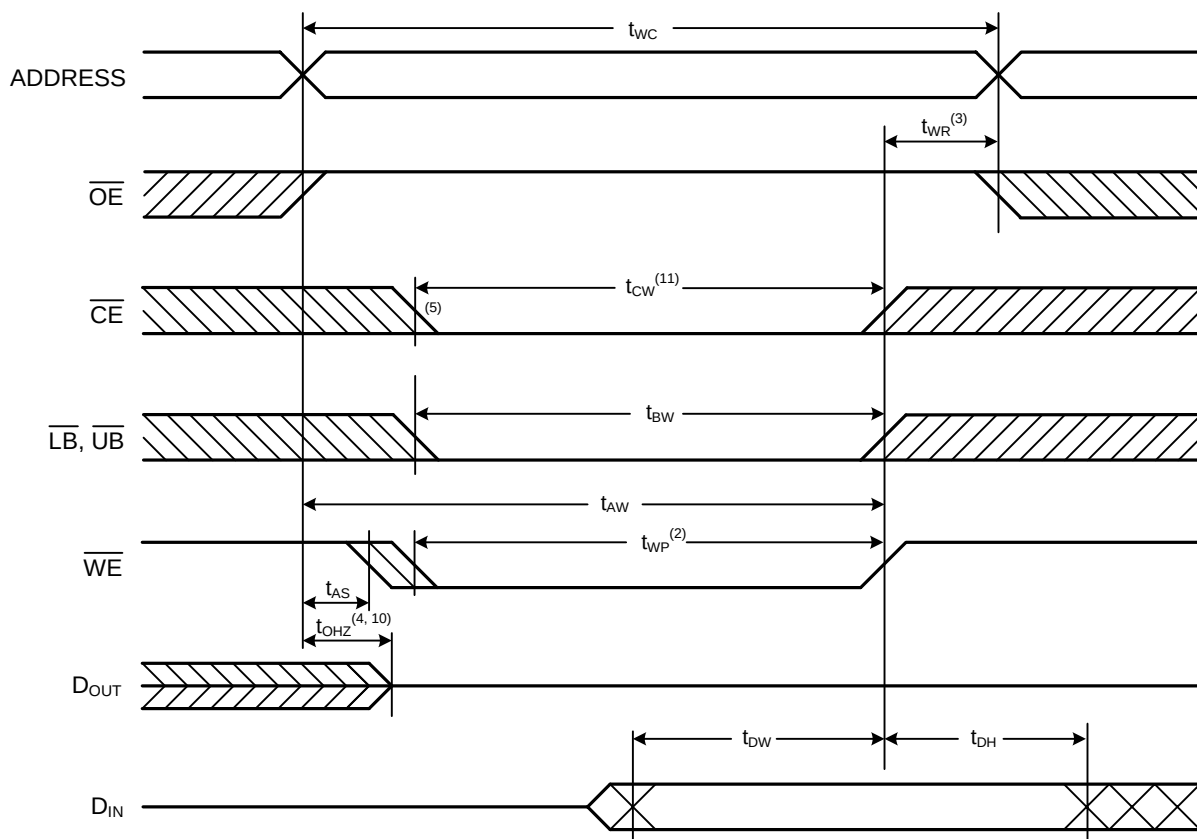
AC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

WRITE CYCLE

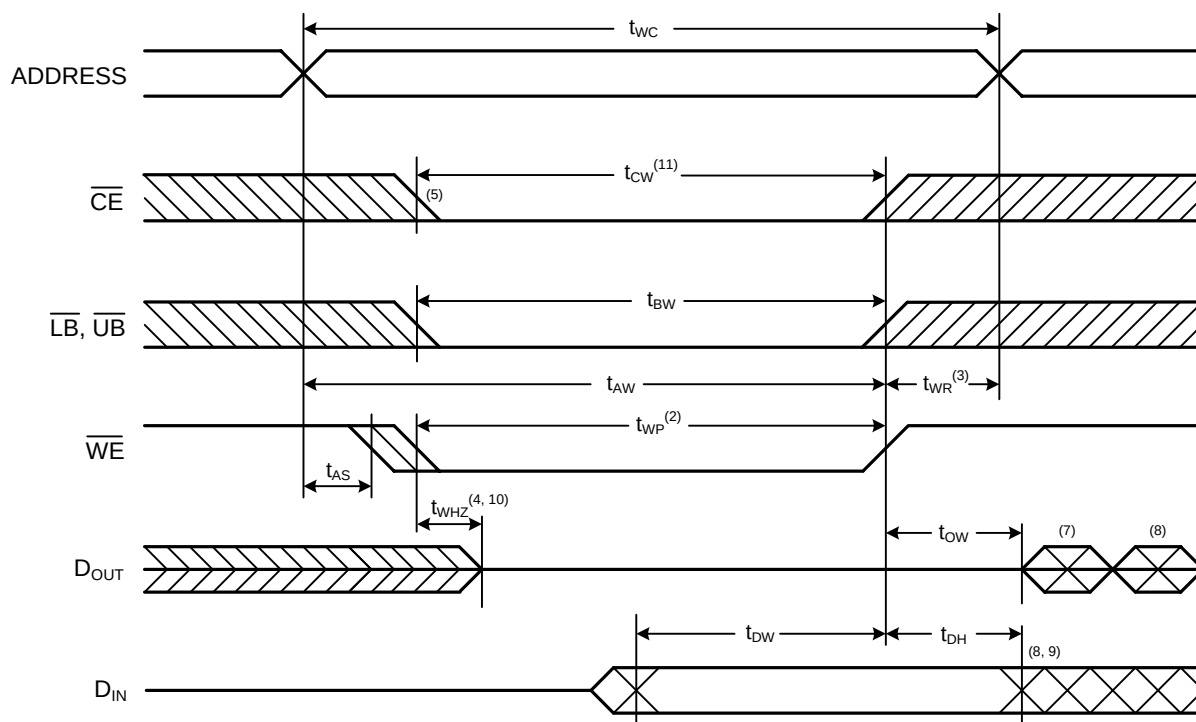
| JEDEC<br>PARAMETER<br>NAME | PARAMETER<br>NAME | DESCRIPTION                                                             | CYCLE TIME : 55ns<br>( $V_{CC}=3.0\sim 5.5\text{V}$ ) |      |      | CYCLE TIME : 70ns<br>( $V_{CC}=2.7\sim 5.5\text{V}$ ) |      |      | UNIT |
|----------------------------|-------------------|-------------------------------------------------------------------------|-------------------------------------------------------|------|------|-------------------------------------------------------|------|------|------|
|                            |                   |                                                                         | MIN.                                                  | TYP. | MAX. | MIN.                                                  | TYP. | MAX. |      |
| $t_{AVAX}$                 | $t_{WC}$          | Write Cycle Time                                                        | 55                                                    | --   | --   | 70                                                    | --   | --   | ns   |
| $t_{AVWL}$                 | $t_{AS}$          | Address Set up Time                                                     | 0                                                     | --   | --   | 0                                                     | --   | --   | ns   |
| $t_{AVWH}$                 | $t_{AW}$          | Address Valid to End of Write                                           | 55                                                    | --   | --   | 70                                                    | --   | --   | ns   |
| $t_{ELWH}$                 | $t_{CW}$          | Chip Select to End of Write ( $\overline{CE}$ )                         | 55                                                    | --   | --   | 70                                                    | --   | --   | ns   |
| $t_{BLWH}$                 | $t_{BW}$          | Data Byte Control to End of Write ( $\overline{LB}$ , $\overline{UB}$ ) | 25                                                    | --   | --   | 30                                                    | --   | --   | ns   |
| $t_{WLWH}$                 | $t_{WP}$          | Write Pulse Width                                                       | 30                                                    | --   | --   | 35                                                    | --   | --   | ns   |
| $t_{WHAX}$                 | $t_{WR}$          | Write Recovery Time ( $\overline{CE}$ , $\overline{WE}$ )               | 0                                                     | --   | --   | 0                                                     | --   | --   | ns   |
| $t_{WLQZ}$                 | $t_{WHZ}$         | Write to Output in High Z                                               | --                                                    | --   | 25   | --                                                    | --   | 30   | ns   |
| $t_{DVWH}$                 | $t_{DW}$          | Data to Write Time Overlap                                              | 25                                                    | --   | --   | 30                                                    | --   | --   | ns   |
| $t_{WHDX}$                 | $t_{DH}$          | Data Hold from Write Time                                               | 0                                                     | --   | --   | 0                                                     | --   | --   | ns   |
| $t_{GHQZ}$                 | $t_{OHZ}$         | Output Disable to Output in High Z                                      | --                                                    | --   | 25   | --                                                    | --   | 30   | ns   |
| $t_{WHQX}$                 | $t_{OW}$          | End of Write to Output Active                                           | 5                                                     | --   | --   | 5                                                     | --   | --   | ns   |

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 <sup>(1)</sup>



WRITE CYCLE 2 <sup>(1, 6)</sup>

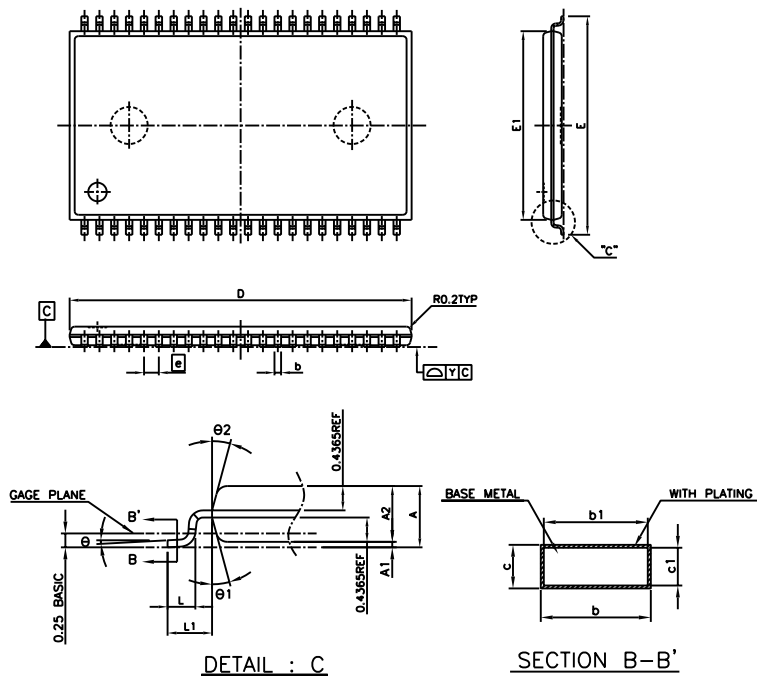


NOTES:

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remains in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE}$  is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L=5\text{pF}$ . The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of write.

PACKAGE DIMENSIONS

【44-TSOP II】



| SYM. | DIMENSION (MM) |       |       | DIMENSION (MIL) |      |      |
|------|----------------|-------|-------|-----------------|------|------|
|      | MIN.           | NOM.  | MAX.  | MIN.            | NOM. | MAX. |
| A    |                |       | 1.20  |                 |      | 47.2 |
| A1   | 0.05           | 0.10  | 0.15  | 2.0             | 3.9  | 5.9  |
| A2   | 0.95           | 1.00  | 1.05  | 37.4            | 39.4 | 41.3 |
| b    | 0.30           |       | 0.45  | 11.8            |      | 17.7 |
| b1   | 0.30           | 0.35  | 0.40  | 11.8            | 14.8 | 15.7 |
| c    | 0.12           |       | 0.21  | 4.7             |      | 8.3  |
| c1   | 0.12           | 0.127 | 0.16  | 4.7             | 5    | 6.3  |
| E1   | 9.96           | 10.16 | 10.36 | 392             | 400  | 408  |
| e    | 0.80 BSC       |       |       | 31.5 BSC        |      |      |
| D    | 18.21          | 18.41 | 18.61 | 717             | 725  | 733  |
| E    | 11.51          | 11.76 | 12.01 | 453             | 463  | 473  |
| L    | 0.40           | 0.50  | 0.60  | 15.7            | 19.7 | 23.6 |
| L1   | 0.80 REF       |       |       | 31.5 REF        |      |      |
| Y    |                |       | 0.075 |                 |      | 3    |
| Ø    | 0°             | 3°    | 6°    | 0°              | 3°   | 6°   |
| Ø1   | 15° REF        |       |       | 15° REF         |      |      |
| Ø2   | 15° REF        |       |       | 15° REF         |      |      |





**Revision History**

| Rev. No. | History                    | Date         |
|----------|----------------------------|--------------|
| 1.0      | Initial draft              | Nov.28, 2006 |
| 1.1      | Modified temperature range | Mar.28,2007  |
|          |                            |              |
|          |                            |              |
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